REMARKS

I. Summary of Office Action

Claims 1-38 are pending in this application.

Claims 31-38 were rejected under 35 U.S.C. § 112 as indefinite.

Claims 1-7, 11, 12, 15-25, 29, and 30 were rejected under 35 U.S.C. § 102(b) as being anticipated by Zhou et al. U.S. Patent No. 6,122,654 (hereinafter "Zhou").

Claims 1, 2, 6 and 14-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by White U.S. Patent No. 4,344,151 (hereinafter "White").

Claims 31, 32, and 38 were rejected under 35 U.S.C. § 102(e) as being anticipated by Brightman et al. Reissued U.S. Patent No. RE39,385.

II. Summary of Applicants' Reply

Claims 1, 4, 24, and 31 have been amended to more particularly define the claimed invention. Claim 34 has been amended to correct a minor typographical error. The Examiner's claim rejections are respectfully traversed. Applicant respectfully requests that these rejections be withdrawn.

III. The § 112 Rejection

Claims 31-38 were rejected under 35 U.S.C. § 112 as indefinite. In particular, the Examiner rejected claim 31 due to a lack of clear antecedent basis for the phrase, "the associated multiplier circuit." Applicant has reworded this portion of claim 31 to obviate this issue. Therefore, applicant respectfully submits that the rejection to independent claim 31, and its dependent claims 32-38, under 35 U.S.C. § 112 should be withdrawn.

III. The § 102 Rejections

A. Claims 1-7, 11, and 12, 14-23

Applicant's amended independent claim 1 is directed to a multi-functional digital signal processor with input adders for selectively adding inputs, multipliers that use the results of the input adders, and output adders for selectively adding the multiplier outputs.

The Examiner contends that FIG. 5 of Zhou shows all the features of applicant's claimed invention. In particular, the Examiner asserts that adder 75 in FIG. 5 of Zhou shows one of applicant's claimed input adder circuitries. However, the inputs to adder 75 are directly connected to registers 61 and 68, and the output of adder 75 is directly connected to the input of multiplier 76. Therefore, since the inputs and outputs of adder 75 are fixed, adder 75 fails to show applicant's claimed feature of an input adder comprising "input selection circuitry for controllably selecting from the inputs" (amended claim 1). The inputs and outputs of the other adders in FIG. 5 are similarly fixed, so Zhou fails to show "at least one of the input adder circuitries compris[ing] input selection circuitry for controllably selecting from the inputs" (amended claim 1).

The Examiner also contends that FIG. 1 of White shows all the features of applicant's claimed invention. However, White also does not show controllably selecting from the inputs. For example, in the top subcircuit of FIG. 1, the inputs to adder 15 are fixed to paths 11 and 12, and the output of adder 15 is fixed to the input of multiplier 26.

This is true of all the adders and multipliers shown in FIG. 1 of White.

Accordingly, applicant has shown that independent claim 1 is allowable. Dependent claims 2-7, 11, 12, and 14-23, which depends from independent 1, are allowable at least because they depend from an allowable claim. Applicant respectfully requests that the rejections of claims 1-7, 11, 12, and 14-23 be withdrawn.

B. Claims 24, 25, 29, and 30

Applicant's independent claim 24 is directed toward DSP circuitry with input adders that operate on controllably selected outputs from registers, multipliers that selectively operate on the outputs of the input adders, and output adders that selectively operate on the outputs of the multipliers. The Examiner contends that FIG. 5 of Zhou shows all the features of applicant's claimed invention. However, applicant's amended claim 24 specifies, among other things, "at least one of the plurality of input adder circuits comprises input selection circuitry for controllably selecting among the signals from the registers." For similar reasons as those stated above in Section A, applicant's amended claim 24 is distinguishable from Zhou. Therefore, independent claim 24 should be allowable. Dependent claims 25, 29, and 30, which depend from allowable independent claim 24, should also be allowable. Applicant respectfully requests that the rejections of claims 24, 25, 29, and 30 be withdrawn.

C. Claims 31, 32, and 38

Applicant's amended independent claim 31 is directed to a plurality of multipliers used in DSP circuitry,

where one set of inputs to the multipliers is obtained by adding register outputs, and another set of inputs is obtained by selecting from register outputs or external circuitry.

The Examiner contends that FIG. 2 of Brighton shows all of the features of applicant's claimed invention. In particular, the Examiner cites multiplier core 58 (FIG. 2) to show applicant's claimed feature of "a plurality of multiplier circuits," and the ADDER INPUT of multiplier core 58 to show "selectively adding outputs of selected ones of the registers" (claim 31). Applicant notes that there is clearly only one multiplier core in White. Furthermore, the input to ADDER INPUT is fixed to register A-LATCH. Therefore, applicant respectfully submits that Brighton neither shows a plurality of multipliers nor "selection circuitry for controllably selecting among the outputs of the registers" (amended claim 31).

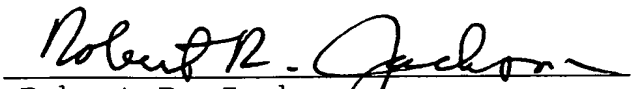
For at least the foregoing reasons, independent claim 31 is allowable. Dependent claims 32 and 38, which depend from claim 31, are allowable at least because they depend from an allowable claim. Applicant respectfully requests that the rejections of claims 31, 32, and 38 be withdrawn.

IV. Conclusion

For at least the reasons set forth above, applicant respectfully submits that this application is in condition for allowance.

Reconsideration in light of the foregoing remarks and a favorable action are respectfully requested.

Respectfully submitted,



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